Amendments to the Claims: This listing of claims will replace all prior versions, and listings, of claims in the application

Listing of Claims:

1. (Currently Amended) A pixel-capture circuit, comprising:

a pixel-capture device having a pixel node and operable to convert light intensity into a pixel signal at the pixel node, the pixel signal representing a captured pixel; ~~and~~

a row node carrying a row signal that is operable to couple the pixel node to a column trace during a read period of the captured pixel and operable to set the pixel node to a predetermined signal level during a reset period; and

a reset node carrying a reset signal that is operable to couple the row node to the pixel node during the reset period,

wherein the row signal changes between predetermined voltage levels during at least one portion of the reset period and sets the pixel node to the predetermined signal level such that the row node is coupled to the pixel node during the reset period.

2. (Currently Amended) The circuit of claim 1, further comprising

a reset trace carrying ~~a~~the reset signal that is operable to uncouple the pixel node from a row trace during the reading of the captured pixel.

3. (Original) The circuit of claim 2 wherein the pixel-capture device is disposed on a silicon substrate.

4. (Original) The circuit of claim 3 wherein the row trace, the column trace, and the reset trace are disposed within no more than two conductive layers disposed on the silicon substrate.

5. (Original) The circuit of claim 1 wherein the pixel-capture device comprises a photodiode.

6. (Original) The circuit of claim 1 wherein the pixel signal comprises a voltage.

7. (Original) The pixel-capture circuit of claim 1, further comprising:

a substrate;

two conductive layers disposed on the substrate; and

one or more conductive paths respectively operable to carry the row signal, each of the conductive paths disposed in a respective one of the two conductive layers.

8. (Previously Presented) The pixel-capture circuit of claim 7 wherein the pixel capture circuit comprises no conductive layers disposed on the substrate other than the two conductive layers.

9. (Currently Amended) A pixel-capture circuit, comprising:

a pixel-capture device having a first node and a second node, the first node coupled to a first supply node;

a first transistor having a control node, a first drive node, and a second drive node, the control node ~~coupled~~connected to the second node of the pixel-capture device and the first drive node coupled to a second supply node;

a second transistor having a control node, a first drive node, and a second drive node, the control node of the second transistor ~~coupled~~ connected to a row node, the first drive node of the second transistor ~~coupled~~connected to the second drive node of the first transistor, the second drive node of the second transistor ~~coupled~~directly connected to a column node; and

a third transistor having a control node, a first drive node, and a second drive node, the control node of the third transistor coupled to a reset node, the first drive node of the third transistor ~~coupled~~connected to the row node, the second drive node of the third transistor ~~coupled~~connected to the second node of the of the pixel-capture device,

wherein the row node carries a row signal, the row signal changes between predetermined levels during at least one portion of ~~the~~a reset period.

10. (Original) The circuit of claim 9 wherein the first, second, and third transistors comprise MOSFET transistors.

11. (Currently Amended) A CMOS array comprising:

a plurality of pixel-capture circuits arranged in rows and columns, pixel-capture circuit comprising:

a pixel-capture device having a pixel node and operable to convert light intensity into a pixel signal at the node, the pixel signal representing a captured pixel; ~~and~~

a row node carrying a row signal that is operable to couple the pixel node to a column trace during a read period of the captured pixel and operable to set the node to a predetermined signal level during a reset period; and

a reset node carrying a reset signal that is operable to couple the row node to the pixel node during the reset period,

wherein the row signal changes between predetermined levels during at least one portion of the reset period and sets the pixel node to the predetermined signal level during the reset period such that the row node is coupled to the pixel node during the reset period.

12. (Currently Amended) The CMOS array of claim 11, further comprising a reset trace carrying ~~a~~ the reset signal that is operable to uncouple ~~a~~the pixel node from the row trace during the reading of the captured pixel.

13. (Original) The CMOS array of claim 12, further comprising a first conductive layer having the row trace and the reset trace disposed therein and a second conductive layer having the column trace disposed therein.

14. (Currently Amended) A system comprising:

a CMOS array having:

a plurality of pixel-capture circuits arranged in rows and columns, pixel-capture circuit comprising:

a pixel-capture device having a pixel node and operable to convert light intensity into a pixel signal at the pixel node, the pixel signal representing a captured pixel; and

a row node carrying a row signal that is operable to couple the pixel node to a column trace during a read period of the captured pixel and operable to set the pixel node to a predetermined signal level during a reset period; and

a reset node carrying a reset signal that is operable to couple the row node to the pixel node during the reset period,

a processor coupled with the CMOS array and operable to facilitate ~~the~~ detection of a voltage signal at each column trace in each pixel in the CMOS array,

wherein the row signal changes between predetermined levels during at least one portion of the reset period and sets the pixel node to the predetermined signal level such that the row node is coupled to the pixel node during the reset period.

15. (Original) The system of claim 14, further comprising a memory coupled to the processor and operable to store the pixel signal.

16. (Currently Amended) A method, comprising:

integrating an amount of light;

generating a light level signal on a pixel node, the pixel node signal having a level related to the integrated amount of light;

generating a first control signal on a first control node;

generating a second control signal on a second control node to control ~~the~~ resetting of the light level signal;

reading the light level signal in response to the control signal on ~~a~~the first control node; and

resetting a level of the light level signal at the pixel node in response to the second control signal, wherein the resetting of the signal level occurs during a reset period and includes connecting the first control node to the pixel node via a switching device and driving the

resetting of the level of the light level signal using the first control signal, the first control signal changing between predetermined levels during at least one portion of the reset period.

17. (Currently Amended) The method of claim 16, wherein ~~the:~~the reading of the light level signal comprises detecting a level at ~~a~~the second control node.

18. (Currently Amended) The method of claim 16 wherein the driving of the resetting of the level of the light level signal comprises:

setting a level at ~~the~~another control node to a predetermined high level; and

pulsing the level at the first control node to a predetermined low level from the predetermined high level, the predetermined high level being higher than the predetermined low level.

19. (Currently Amended) The circuit of claim 1, further comprising:

a reset transistor for controlling ~~the~~ reset of the pixel signal at the pixel node of the pixel capture device, the reset transistor being controlled by ~~a~~ the reset signal from ~~a~~ the reset node, the reset transistor connecting the row signal to the pixel node during the reset period and disconnecting the row signal from the pixel node during the image-capture period; and

a row selection transistor,

wherein the row node is coupled to the reset transistor to selectively couple the row node to the pixel node of the pixel capture device for reset and the row node is further coupled to the row selection transistor to control the row selection transistor to selectively couple the pixel node of the pixel capture device to ~~a~~ the column trace for readout.

20. (New) The circuit of claim 19, wherein:

the row selection transistor couples the pixel node of the pixel capture device to the column trace during the readout period and uncouples the pixel node from the column trace during the image-capture period; and

a further transistor connected between the pixel capture device and the row selection transistor, the row select transistor being disposed between the further transistor and the column trace.